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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/824,219	04/13/2004	Shumpei Kawasaki	101-9409J	6297

7590 01/09/2008

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EXAMINER	
CHANKONG, DOHM	

ART UNIT	PAPER NUMBER
2152	

MAIL DATE	DELIVERY MODE
01/09/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/824,219	KAWASAKI ET AL.	
	Examiner	Art Unit	
	Dohm Chankong	2152	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 October 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *23-41* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *23-41* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1> This action is in response to Applicant's amendment, filed on 10.15.2007. Claims 17-22 are canceled. Claims 1-16 were previously canceled. Claims 23-41 are added. Thus, claims 23-41 are presented for further examination.

2> This is a final rejection.

Response to Arguments

3> Applicant's arguments with respect to claims 23-41 have been considered but are moot in view of the new ground(s) of rejection necessitated by Applicant's amendment.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4> Claims 23-37, 40 and 41 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

a. Specifically, the independent claims 23, 32, 37, and 41 recite, in part, a "graphics processing module" or a "image processing accelerator" that processes image data.

Applicant's specification does not describe a single processing module for processing data. Rather, Applicant's specification describes using a first and second bus and a multiple, arithmetic and divide unit that perform calculations in parallel to provide image processing [Applicant's published patent application 20040199716, 0014]. Furthermore, Applicant's specification states that image processing is carried out by a microprocessor that comprises the aforementioned units attached to the various buses, peripheral modules also attached to the bus, and a bus state controller [0360].

The peripheral modules are described as an "interrupt controller INTC, a dynamic memory access controller DMAC, a divider unit DIVU, a free running timer FRT, a watch-dog timer WDT and a serial communication interface SCI" [0089]. There is no discussion of a single graphics module that performs image processing as claimed.

Thus, the independent claims contain subject matter that was not described in the specification to reasonably convey that Applicant had possession of the claimed invention.

b. Dependent claims are rejected based on their dependency on their parent claims. Additionally, some fail to comply with the written description as well. For example, claim 25 recites the graphics processing module for performing coordinate transformation. Applicant's specification describes that coordinate transformation takes place at the CPU and the multiplier unit [0207]. Even if the multiplier unit were interpreted as the graphics module, the specification clearly states that the CPU helps

perform the function as well. Thus, the claimed limitation lacks proper written description.

c. Similarly, claim 33 recites an image processing accelerator that includes a divider. However, Applicant's specification does not describe the divider unit as being part of any accelerator or module. The divider unit seems to be its own separate unit on the microprocessor.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5> Claims 23, 24, 28-32, 35, and 37-41 are rejected under 35 U.S.C §103(a) as being unpatentable over Leach et al, U.S Patent No. 5.179.689 ["Leach"].

6> As to claims 23, Leach discloses a microprocessor comprising:

a central processing unit fetching and executing instructions [Figure 1 | column 4 «lines 13-18»];

a graphics processing module processing image data [column 2 «lines 12-17» | column 6 «lines 60-62» : Leach's multiplier is interpreted as a graphics processing module | column 7 «lines 16-40»];

an external interface module [column 3 «lines 16-30» : accessing external memory using the DMA controller] and

a plurality of terminals including a clock terminal [column 15 «lines 52-68»],

wherein said central processing unit includes a plurality of registers [column 6 «lines 63-64»],

wherein said external interface module outputs a control signal for coupling to an external synchronous memory [column 5 «lines 8-16» | column 14 «lines 29-34»],

wherein said central processing unit is operable to access said external interface module for accessing said external synchronous memory [column 3 «lines 16-30» : CPU accesses the DMA controller], and

wherein said microprocessor outputs a clock signal via said clock terminal for coupling to said external synchronous memory [column 14 «line 64» to column 15 «line 25»].

7› As to claim 24, Leach discloses said graphics processing module is operable to provide three-dimensional image processing [column 2 «lines 12-17»].

8› As to claim 28, Leach further discloses:

a cache memory, wherein said cache memory includes an instruction cache module and a data cache module [Figure 7 «item 150» : buffer corresponding to a data cache | column 2 «lines 61-66» | column 3 «lines 22-29» | column 27 «lines 31-40»].

9› As to claim 29, Leach further discloses:

a direct memory access controller including a first register and a second register [Figure 1 «item 22»], wherein said first register contains a starting address, and wherein said second register contains a transfer address [column 29 «lines 50-56»].

10› As to claim 30, Leach further discloses:

a direct memory access controller including a plurality of registers, wherein said plurality of registers of the direct memory access controller include a control register and an address register [column 8 «lines 1-29»].

11› As to claim 31, Leach further discloses:

a clock module including a PLL circuit, wherein said clock module is operable to multiple a frequency by two times or four times [column 15 «line 52 to column 16 «line 26»]

12› As to claims 32, 37 and 41, Leach discloses a microprocessor comprising:

a central processing unit [Figure 1 | column 4 «lines 13-18»];

a three-dimensional image processing accelerator [column 2 «lines 12-17» | column 6 «lines 60-62»];

a direct memory access controller [column 8 «lines 1-29»];

an external interface module coupled to said CPU, said three-dimensional image processing accelerator and said direct memory access controller [Figure 1 | column 3 «lines 16-30»] and

a plurality of terminals including a clock terminal [column 15 «lines 52-68»],

wherein said central processing unit includes a plurality of registers [column 6 «lines 63-64»],

wherein said external interface module outputs a control signal for coupling to an external synchronous memory [column 5 «lines 8-16» | column 14 «lines 29-34»],

wherein said central processing unit is operable to access said external interface module for accessing said external synchronous memory [column 3 «lines 16-30» : CPU accesses the DMA controller], and

wherein said microprocessor outputs a clock signal via said clock terminal for coupling to said external synchronous memory [column 14 «line 64» to column 15 «line 25»].

13> As to claim 35, Leach discloses said direct memory access controller is operable to transfer data between said external synchronous dynamic memory and said memory [column 3 «lines 16-30»].

14> As to claim 36, it is rejected for the same reasons as set forth for claim 27.

15> As to claims 38 and 39, Leach discloses a microprocessor comprising:

a central processing unit [Figure 1 | column 4 «lines 13-18»];

a memory [Figure 1];

a peripheral module [column 2 «lines 12-17» | column 6 «lines 60-62»];

a direct memory access controller coupled to said peripheral module[column 8 «lines 1-29»];

an external interface module for coupling to an external synchronous dynamic memory with a plurality of memory banks [Figure 1 | column 3 «lines 16-30»];

wherein said direct memory access controller includes a first register for storing a source address, a second register for storing a destination address, and a third register for storing control information [column 29 «lines 50-56»],

wherein said peripheral module is operable to output a transfer request to said direct memory access controller [column 19 «lines 13-28»], and

wherein said direct memory access controller is operable to transfer data between said external synchronous dynamic memory and said peripheral module [column 29 «line 50» to column 30 «line 35»].

16› As to claim 40, Leach further discloses:

a three-dimensional image processing accelerator coupled to said central processing unit, wherein said external bus interface is operable to output image data processed by said three-dimensional image processing accelerator to said external synchronous dynamic memory [column 6 «line 60» to column 7 «line 15»].

17› Claims 25, 26, 34, and 35, are rejected under 35 U.S.C §103(a) as being unpatentable over Leach, in view of Murata et al, U.S Patent No. 5.615.322 ["Murata"].

18› As to claims 25, 26, 34, and 35, Leach does disclose using the microprocessor for image processing but does not expressly disclose coordinate transformation processing or

perspective transformation processing. However, such functionality was well known in the art at the time of Applicant's invention.

For example, Murata discloses a microprocessor directed to three-dimensional image processing [abstract | Figure 1A «item 16»] that performs both coordinate transformation and perspective transformation processing [Figure 1a «items 18 and 20»]. It would have been obvious to one of ordinary skill in the art to adapt Leach's microprocessor to include the coordinate transformation and perspective transformation processing components taught by Murata. The components would improve Leach by enabling faster processing of 3-d images.

19› Claims 27 and 36 are rejected under 35 U.S.C §103(a) as being unpatentable over Leach in view of Okada, U.S Patent No. 5.134.391.

20› As to claim 27, Leach does not expressly disclose outputting data resulting from three-dimensional image processing to an external LCD device via said terminals. However, Leach does disclose that the data processing device may be used for graphics applications and to provide video display refresh functionality [column 19 «lines 47-50»]. Additionally, Okada discloses outputting data resulting from 3-d image processing to an external LCD device [Figure 4 «items 14»]. One of ordinary skill in the art would have reasonably interpreted this disclosure as referring to outputting the data to a monitor display of a computer. LCD monitors were also well known in the art at the time of Applicant's invention.

Therefore, it would have been obvious to one of ordinary skill in the art to have attached Leach's data processing chip to an LCD display to output the data of the three-

dimensional image processing. One of ordinary skill in the art would have been motivated to do so because it was well known at the time of Applicant's invention to attach LCD displays to graphical chips such as the one disclosed in Leach.

21> Claim 33 is rejected under 35 U.S.C §103(a) as being unpatentable over Leach, in view of Lentz et al, U.S Patent No. 5.533.185.

22> As to claim 33, Leach discloses a microprocessor used for image processing but does not disclose a divider. However, such a feature in graphics microprocessors was well known in the art at the time of Applicant's invention. For example, Lentz discloses a graphics processor that contains a divider [column 10 «lines 7-23» : divider register]. Thus, it would have been obvious to one of ordinary skill in the art to have reasonably inferred that Leach's image processing microprocessor would contain a divider to perform the necessary computations as taught by Lentz.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

Pelham et al, U.S Patent No. 4.967.375 ;

Kiuchi, U.S Patent No. 5.440.747;

Mical et al, U.S Patent No. 5.572.235;

Souviron, U.S Patent No. 5.612.714.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, THIS ACTION IS MADE FINAL. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dohm Chankong whose telephone number is 571.272.3942. The examiner can normally be reached on Monday-Friday [8:30 AM to 4:30 PM].

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bunjob Jaroenchonwanit can be reached on 571.272.3913. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

DC
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1/7/8